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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/511,437	10/25/2004	Hiroshi Takahara	259686US2PCT	3978

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EXAMINER	
CHOWDHURY, AFROZA Y	
ART UNIT	PAPER NUMBER
2609	

SHORTENED STATUTORY PERIOD OF RESPONSE	NOTIFICATION DATE	DELIVERY MODE
3 MONTHS	03/02/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Notice of this Office communication was sent electronically on the above-indicated "Notification Date" and has a shortened statutory period for reply of 3 MONTHS from 03/02/2007.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/511,437	TAKAHARA, HIROSHI	
	Examiner	Art Unit	
	Afroza Y. Chowdhury	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-12 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-12 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 10/252004, 11/1/2005.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figure 46 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. Applicant is reminded of the proper language and format for an **abstract** of the disclosure.

The abstract should be in narrative form and generally limited to **a single paragraph** on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

3. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required:

Regarding claim 4, "an **aggregation circuit** configured to aggregate image data or data equivalent to image data; and a **conversion circuit** configured to convert aggregation results produced by the aggregation circuit into a start pulse signal for the gate driver circuit."

Regarding claim 5, "the control method comprising: **generating a delay time** when **changing the ratio between the non-display and display areas on the screen** from a first ratio to a second ratio. However, it would be obvious to generate a delay time when changing the ratio between the non-display and display areas on the screen from a first ratio to a second ratio."

Claim Objections

4. Claim 11 is objected to because of the following informalities: the given condition in claim 11 is missing a parenthesis. Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1, 4, and 6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1, line 5 and claim4, lines 10 - 11, "**aggregating image data or data equivalent to image data**" is not clear. What does aggregating image data means? What does data equivalent to image data means?

Claim 1, lines 6-8, "**turning off the switching element for a longer period if the aggregated data is large in amount than if the aggregated data is small in amount.**" It is not clear turning off switching element. It seems that the switching element should be turning "on" when there is larger data instead of "off."

Claim 4, lines 10-14, "**a conversion circuit configured to convert aggregation results produced by the aggregation circuit into a start pulse signal for the gate driver circuit**" is not clear. What does aggregation circuit means?

Regarding claim 6, it is not clear what the inventor meant by "**display area/(the non-display area+the display area on the screen) is from 1/16 to 1/1 both inclusive**". The ratios are not well understood. From 1/16 to 1/1 of what?

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1–8, 10, and 12 are rejected under 35 U.S.C. 102(e) as being unpatentable by Yamano et al. (US 2005/0057580).

As to claim 1, Yamano et al. teaches a drive method of an EL display apparatus that comprises a switching element which turns on and off a current path between a driver transistor and an EL element, in each pixel, the drive method comprising:

aggregating image data or data equivalent to image data (page 9, [0225]); and turning off the switching element for a longer period if the aggregated data is large in amount than if the aggregated data is small in amount (page 10, [0233] – [0234], [0236] – [0237], page 12, [0259], fig. 38), as best understood.

As to claim 2, Yamano et al. discloses an EL display apparatus comprising: a display panel in which EL elements are formed in a matrix (page 3, [0038], fig. 6, [0261]); and a source driver circuit configured to supply programming current to the display panel (page 12, [0261], fig. 44, page 34, [0498]),

wherein the source driver circuit comprises an output stage that has a plurality of unit current elements (fig. 63, page 43, [0615]) and a variable circuit configured to

control current flowing from the unit current elements (page 10, [0236] – [0237], fig. 4, page 12, [0259], pages 43,[0613] – [0615], fig. 63).

As to claim 3, Yamano et al. teaches a drive method of an EL display apparatus that includes a moving-picture detection circuit that detects moving pictures and a feature extraction circuit that extracts features of video images, the drive method of the EL display apparatus comprising:

first changing a number of selected pixel rows depending on output data from the moving-picture detection circuit (page 18, [0337], fig.1, 2, 38,); and

second changing the number of selected pixel rows depending on output data from the feature extraction circuit (page 18, [0327], fig.1, 2, 38, and page 72, [0911]).

As to claim 4, Yamano et al. discloses an EL display apparatus that controls brightness of a screen using a ratio between non-display and display areas on the screen, the EL display apparatus comprising:

a display area in which EL elements ([0059]) and driver transistors that drive the EL elements are formed in a matrix ([0060]);

gate signal lines configured to transmit voltages that turn on and off the EL elements in each pixel row (fig. 40, page 35, [0505], [0506]); a gate driver circuit configured to drive the gate signal lines (fig. 40, page 35, [0504]).

an aggregation circuit configured to aggregate image data or data equivalent to image data (page 9, [0021], [0225], fig. 1, page 41, [0585], [0587]); and a conversion

circuit configured to convert aggregation results produced by the aggregation circuit into a start pulse signal for the gate driver circuit (page 13, [0268], [0273] – [0274], [0276], fig. 1 and fig. 8), as best understood.

As to claim 5, Yamano et el. discloses a control method of an EL display apparatus that controls brightness of a screen using a ratio between non-display and display areas on the screen, the control method comprising: generating a delay time when changing the ratio between the non-display and display areas on the screen from a first ratio to a second ratio (page 17, [0318] – [0320]).

As to claim 6, Yamano et al teaches a drive method of an EL display apparatus wherein the display area/(the non-display area+the display area on the screen) is from 1/16 to 1/1 both inclusive (page 17, [0322], page 42, [0606], and page 52, [0711].)

As to claim 7, Yamano et al. teaches an EL display apparatus comprising: a display panel in which each pixel contains a capacitor (page 35, [0512]), an EL element, and a P-channel driver transistor configured to supply current to the EL element (fig. 1, [0063], [0071]), and

wherein the pixels are arranged in a matrix (page 3, [0095]); and a source driver circuit configured to supply programming current to the display panel (page 12, [0261], fig. 44, page 34, [0498]),

wherein the source driver circuit comprises an output stage that has an N-channel unit transistor configured to output a plurality of unit currents (fig. 72, page 43, [0610], page 46, [0648]).

As to claim 8, Yamano et al. discloses an EL display apparatus wherein a capacitance of a capacitor is Cs (pF) and one pixel occupies an area of S (square μm), and a condition $500/S \leq Cs \leq 20000/S$ is satisfied (page 9. [0223]).

As to claim 10, Yamano et al. teaches an EL display apparatus wherein a number of gradations is K and a size of the unit transistor is St (square μm), and conditions $40 \leq K/\sqrt{\sqrt{(St)}}$ and $St \leq 300$ are satisfied (page 2, [0024], page 3, [0051], page 46, [0640], [0641]).

As to claim 12, Yamano et al. discloses an EL display apparatus comprising: a first EL display panel including a first display screen (fig. 8); a second EL display panel including a second display screen (fig. 8); and

a flexible board configured to connect source signal lines of the first EL display panel with source signal lines of the second EL display panel (fig. 8, page 13, [0273]),

wherein a channel width of driver transistors that drive pixels is W (μm) and a channel length is L (μm), and W/L differs between the driver transistor that drives pixels in the first display screen and the driver transistor that drives pixels in the second display screen.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claim 9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamano et al. (US 2005/0057580).

As to claim 9, Yamano et al. teaches that the programming current is N times as high as a predetermined value, and the predetermined value is not a fixed value unless white raster display is given (fig. 15, page 19, [0340]). He does not explicitly teaches the condition (A.x.B)/20≤1≤(A.x.B) where pixel size is A (square mm) and predetermined white raster display brightness is B (nt), and a programming current I (μA) from the source driver circuit. However, it would have been obvious for the programming current to satisfy similar condition.

As to claim 11, Yamano et al. teaches output current variations vs transistor size ([fig. 117]) and relationship between gray scale gradiation K and transistor size (page 42, page 46, [0640], page 56, [0746], page 57, [0754]). He does not explicitly disclose an EL display apparatus wherein a number of gradations is K, channel length of the unit

transistor is L (μm), and channel width is W (μm), and a condition ($\sqrt{(K/16)}$) $\leq L/W \leq \sqrt{\sqrt{(K/16)}}x20$ is satisfied. However, it would have been obvious to develop similar condition since channel current depends on (L/W) and there is a relation between K and transistor size.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Afroza Y. Chowdhury whose telephone number is 571-270-1543. The examiner can normally be reached on 7:30-5:00 EST, 5/4/9.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on 571-272-2600. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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SUPERVISORY PATENT EXAMINER